CLAIMS

X There are no amendments to the claims.

___ A complete listing of all claims ever present in this case in ascending order with status identifier is presented in a separate section.

COMPLETE LISTING OF CLAIMS

IN ASCENDING ORDER WITH STATUS INDICATOR

Claims 1-8 (canceled)

9. (original): A memory device comprising:

a gate stack;

a vertical oxide spacer adjacent to said gate stack; and

a continuous nitride layer overlaying said vertical oxide spacer and said gate stack.

10. (original): The memory device of claim 9, wherein said gate stack comprises a floating gate and a control gate.

11. (original): The memory device of claim 9, wherein said vertical oxide spacer is between about 50Å and about 300Å in thickness.

12. (original): The memory device of claim 9, wherein said vertical oxide spacer is about 100Å and about 200Å in thickness.

13. (original): The memory device of claim 9, wherein said nitride layer has a thickness equal to about one half the width of said vertical oxide spacer.

14. (original): A memory device comprising:

a gate stack;

a vertical spacer adjacent to said gate stack, wherein said vertical spacer has a lower portion comprising an oxide and an upper portion comprising a nitride; and

a continuous nitride layer overlaying said vertical spacer and said gate stack.

15. (original): The memory device of claim 14, wherein said vertical oxide spacer is between about 50Å and about 300Å in thickness.

16. (original): The memory device of claim 15, wherein said vertical oxide spacer is between about 100Å and about 300Å in thickness.

17. (original): The memory device of claim 14, wherein said nitride layer has a thickness equal to about one half the width of said vertical oxide spacer.

18. (original): The memory device of claim 14, wherein said gate stack is a flash cell gate stack.

Claims 19-35 (canceled)

36. (original): A memory device comprising:

a gate stack comprising:

a tunnel oxide layer on a substrate;

a floating gate layer over said tunnel oxide layer;

an oxide/nitride/oxide layer over said floating gate layer;

a control gate layer over said oxide/nitride/oxide layer;

a silicide layer over said control gate layer;

a cap over said silicide layer;

a vertical spacer adjacent to said gate stack, wherein said vertical spacer has a lower portion comprising an oxide and an upper portion comprising a nitride; and

a continuous nitride layer overlaying said vertical spacer and said gate stack.

37. (original): The memory device of claim 36, wherein said silicide layer comprises tungsten.

38. (original): The memory device of claim 36, wherein said floating gate layer comprises a polysilicon.

39. (original): The memory device of claim 36, wherein said control gate layer comprises a polysilicon.

40. (original): The memory device of claim 36, wherein said oxide/nitride/oxide layer comprises a silicon nitride layer interposed between two silicon dioxide layers.

41. (original): The memory device of claim 36, wherein said cap comprises nitride.

42. (original): The memory device of claim 36, wherein said cap comprises TEOS.

43. (original): The memory device of claim 36, wherein said oxide portion comprises TEOS.

44. (original): The memory device of claim 36, wherein said vertical spacer is between about 50Å and 300Å in thickness.

45. (original): The memory device of claim 44, wherein said vertical spacer is about 100Å and 200Å in thickness.

46. (original): The memory device of claim 36, wherein said continuous nitride layer has a thickness equal to about one half the width of said vertical spacer.

47. (original): A memory device comprising:

a gate stack comprising:

a tunnel oxide layer on a substrate;

a control gate layer over said tunnel oxide layer;

a silicide layer over said control gate layer;

a cap over said silicide layer;

a vertical spacer adjacent to said gate stack, wherein said vertical spacer has a lower portion comprising an oxide and an upper portion comprising a nitride; and

a continuous nitride layer overlaying said vertical spacer and said gate stack.

Claims 48-56 (canceled)

57. (original): A processor system comprising:

a processor; and

a memory device coupled to exchange data with said processor, said memory device comprising:

a gate stack;

a vertical spacer adjacent to said gate stack, wherein said vertical spacer has a lower portion comprising an oxide and an upper portion comprising a nitride; and

a continuous nitride layer overlaying said vertical spacer and said gate stack.

58. (original): The processor system of claim 57, wherein said vertical oxide spacer is between about 50Å and about 300Å in thickness.

59. (original): The processor system of claim 58, wherein said vertical oxide spacer is between about 100Å and about 300Å in thickness.

60. (original): The processor system of claim 57, wherein said nitride layer has a thickness equal to about one half the width of said vertical oxide spacer.

61. (original): The processor system of claim 57, wherein said gate stack is a flash cell gate stack.